



EST7502B PC Power Supply PWM with Supervisor

GENERAL DESCRIPTION

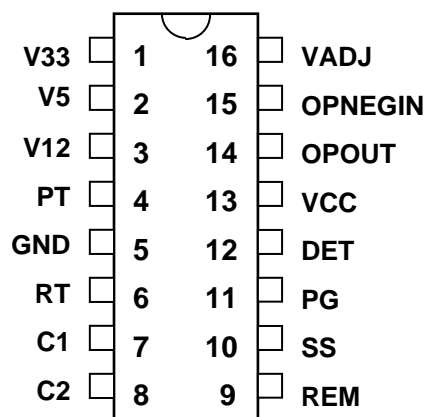
The EST7502B is a pulse-width modulation (PWM) control circuit with complete protection circuits for used in the SMPS (Switched Mode Power Supply). It contains various functions, which are Over Voltage Protection, Under Voltage Protection, Power Good Output (PGO), Remote On/Off control and etc. It can minimize external components of switching power supply systems in personal computer.

Over Voltage Protection (OVP) monitors 3.3V, 5V, 12V and PT input voltage level. Under Voltage Protection (UVP) monitors 3.3V, 5V and 12V input voltage level. Power Good Output monitors the voltage level of power supply.

FEATURES

- Complete PWM Control and Protection Circuitry
- Over Voltage Protection for 3.3V / 5V / 12V / PT
- Under Voltage Protection for 3.3V / 5V / 12V
- 280ms PG Time Delay
- Power Good Output is Open Drain Output
- PWM Control Output are Open Drain Output
- 280 ms Time Delay for UVP
- Remote ON/OFF function De-bounce Time
- Soft-Start function built-in
- 16-Pin Dual In-line Package

PIN CONFIGURATION



ORDERING INFORMATION

ORDER NUMBER	Package	Shipping	Top Marking
EST7502B	DIP 16		



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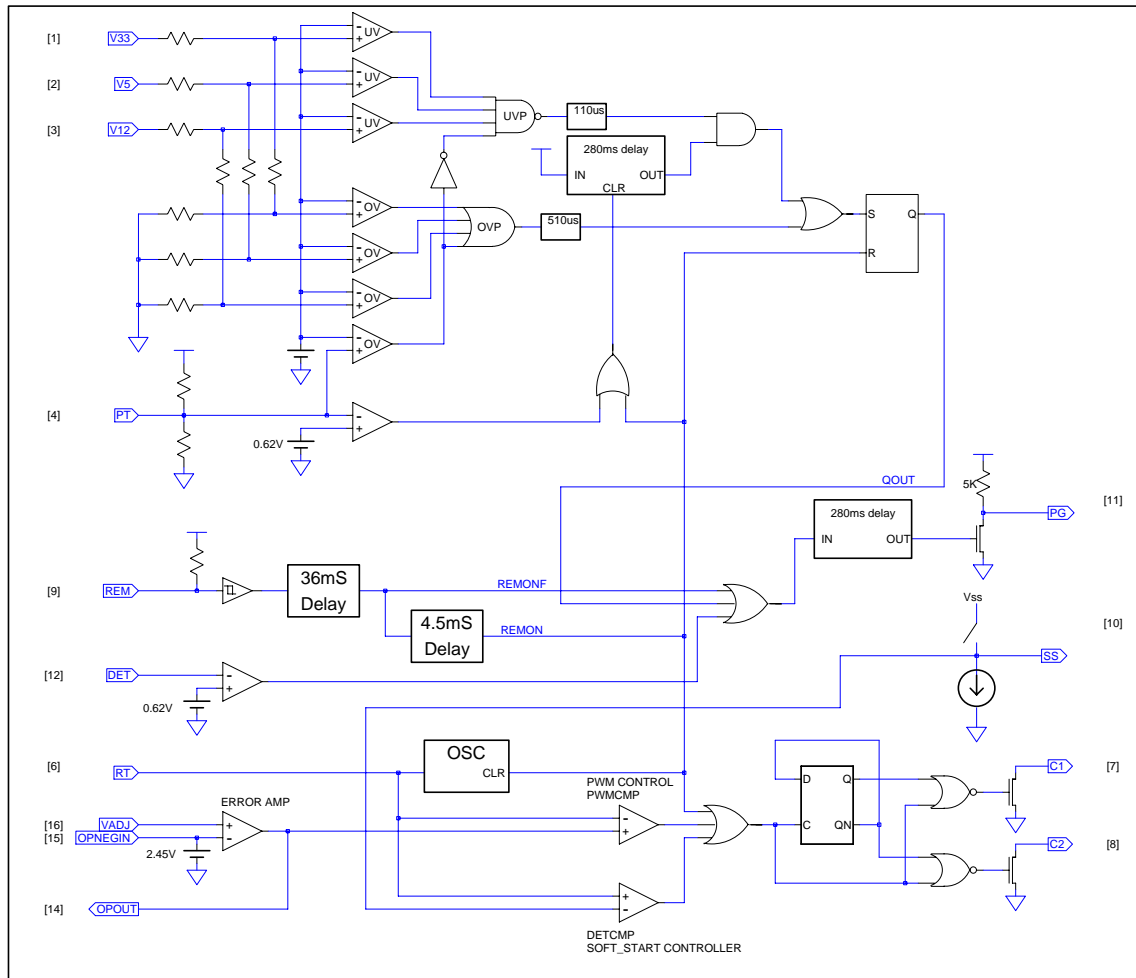
PIN DESCRIPTION

Pin No.	Pin Name	TYPE	FUNCTION
1	V33	I	OVP/UVF input FOR 3.3V.
2	V5	I	OVP/UVF input for 5V.
3	V12	I	OVP/UVF input for 12V.
4	PT	I	Extra OVP protection input.
5	GND	P	Ground.
6	RT	O	Oscillation frequency set by external resistor.
7	C1	O	PWM open drain output 1.
8	C2	O	PWM open drain output 2.
9	REM	I	Remote on/off input. REM="low" that means the main SMPS is turned-on. REM="high", the main SMPS is turned-off.
10	SS	O	Soft start function set by external capacitor.
11	PG	O	Power good signal. PG= "high" means "power good". PG= "low" means "power fail".
12	DET	I	Extra protection input.
13	VCC	P	Supply voltage.
14	OPOUT	O	OP compensation output.
15	OPNEGIN	I	OP compensation negative input.
16	VADJ	I	OP compensation positive input , feedback voltage sense input.



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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS, VCC=5.5V

CHARACTERISTICS	SYMBOL	VALUE	Unit
Supply voltage	VCC	5.5	V
Drain output voltage	Vcc1, Vcc2	5.5	V
Drain output current	Icc1, Icc2	200	mA
Power dissipation	Pd	200	mW
Operating temperature	Topr	-20 ~ +85	°C
Storage temperature	Tstg	-65 ~ +150	°C



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ELECTRICAL CHARACTERISTICS, $T_A=25^{\circ}\text{C}$, $V_{CC}=5\text{V}$,

CHARACTERISTICS	SYMBOL	TEST CONDITION	Min.	Typ.	Max.	Unit
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ERROR AMP SECTION

OPEN LOOP VOLTAGE GAIN		0.5V ~ 3.5V	75	85		dB
CROSS OVER POINT		0dB		1000		KHZ
OPNEG BIAS VOLTAGE		OPNEG OPEN	2.40	2.45	2.50	V
POWERSUPPLY REJECTION RATIO	PSRR		45			dB

OUTPUT SECTION

OUTPUT SATURATION VOLTAGE	Vdssat	Id=200mA		1.1	1.3	V
DRAIN OFF-STATE CURRENT	Idoff	Vcc=Vd=Vs=0V		2	10	uA
RISING TIME	Tr			100	200	ns
FALLING TIME	Tf			50	200	ns

PROTECTION SECTION

OVER VOLTAGE PROTECTION (OVP)	V33		3.8	4.1	4.3	V
	V5		5.8	6.2	6.6	V
	V12		4.4	4.6	4.9	V
	PT		1.23	1.28	1.33	V
	Tg.ov			510		us
UNDER VOLTAGE PROTECTION (UVP)	V33		1.7	1.9	2.2	V
	V5		2.7	3.0	3.3	V
	V12		2.1	2.4	2.7	V
	Tg.uv			120		us
UVP DISABLE VOLTAGE	PT		0.55	0.62	0.68	V
UVP DELAY TIME	Td.uvp		100	280	380	ms

REMOTE ON/OFF SECTION

REM HIGH INPUT VOLTAGE	Vremh		1.8			V
REM LOW INPUT VOLTAGE	Vreml				0.7	V
REM PULL HIGH VOLTAGE	Vremo		2.0		5.25	V
REM DELAY TIME	Td on/off			40		ms

POWER GOOD SECTION

DETECT INPUT VOLTAGE	Vdet			0.68		V
PG OUTPUT PULL-UP RESISTOR	Rpup, pg			5		K Ω
PG OUTPUT LOAD RESISTOR	Rpg		0.5	1	2	K Ω
PG DELAY TIME			180	280	380	ms
SINK CURRENT	lpg.sink	VPG=0.2V		10		mA

SOFT START SECTION

SINK CURRENT OF SS	Iss.sink	RT=100K Ω		15		uA
SOURCE CURRENT OF SS	Iss.source			310		uA

VCC Under Voltage Lockout(UVLO)

Start-up voltage				4.2		V
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TOTAL DEVICE

STANDBY SUPPLY CURRENT	Icc	REM=5V		10	20	mA
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OSCILLATION SECTION

OSCILLATION FREQUENCY	Fosc	RT=100K Ω	70	75	80	KHZ
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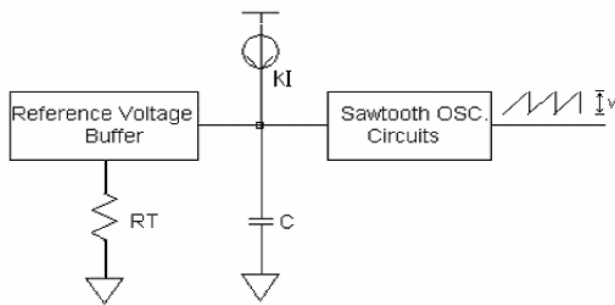
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APPLICATION NOTE

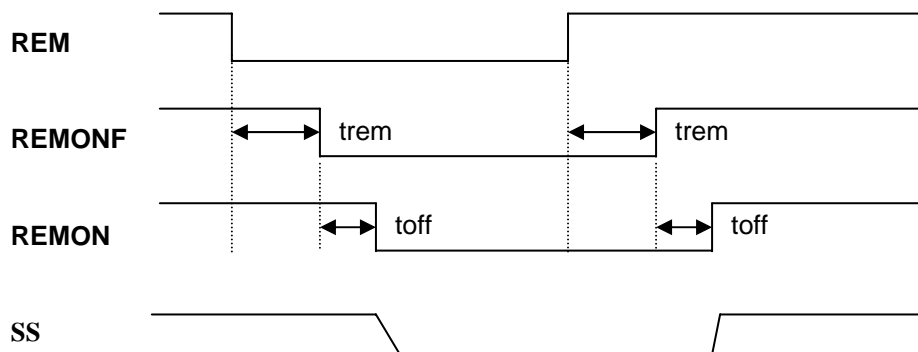
1. Input impedance:

Pin No.	Pin Name	Input impedance
1	V33	52K Ω
2	V5	81K Ω
3	V12	52K Ω
4	PT	24 K Ω +4.6 K Ω

2. Sawtooth OSC. Function:



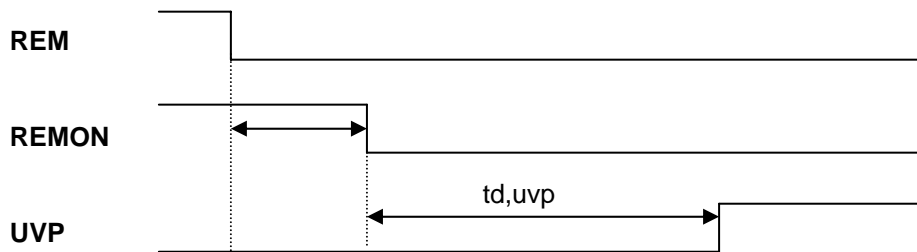
3. REMOTE ON/OFF :





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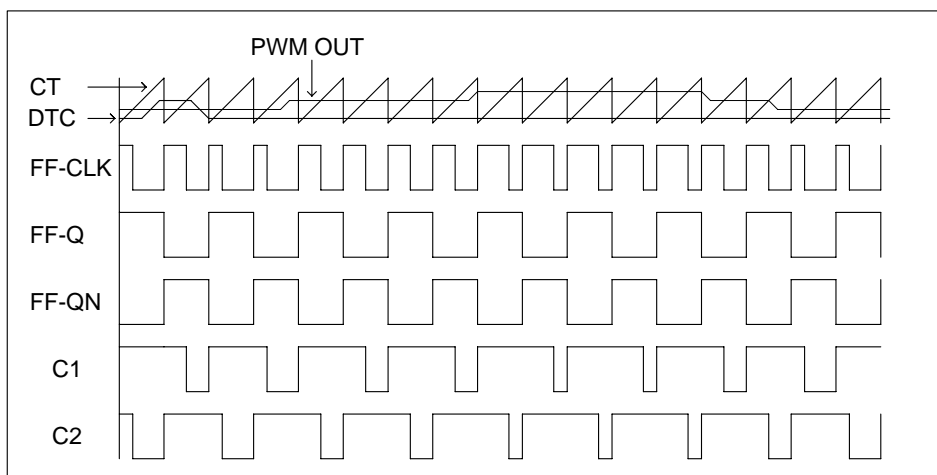
4. Under Voltage Protection Delay Time :



5. Pulse Width Modulation Block :

The output pulse width modulation is generated by comparison of the saw-tooth waveform from the capacitor C_T to the feedback of the voltage.

Therefore, an increase in feedback control signal amplitude cause a linear decrease of the output pulse width. Also, the SS(DTC and Soft-Start) limits the output pulse width. The timing diagram is shown as below:



6. The function of "PT":

This signal is prepared for extra OVP/OPP ($V_{PT} > 1.28V$) or another Disable Under Voltage Protection function ($V_{PT} < 0.62V$)

